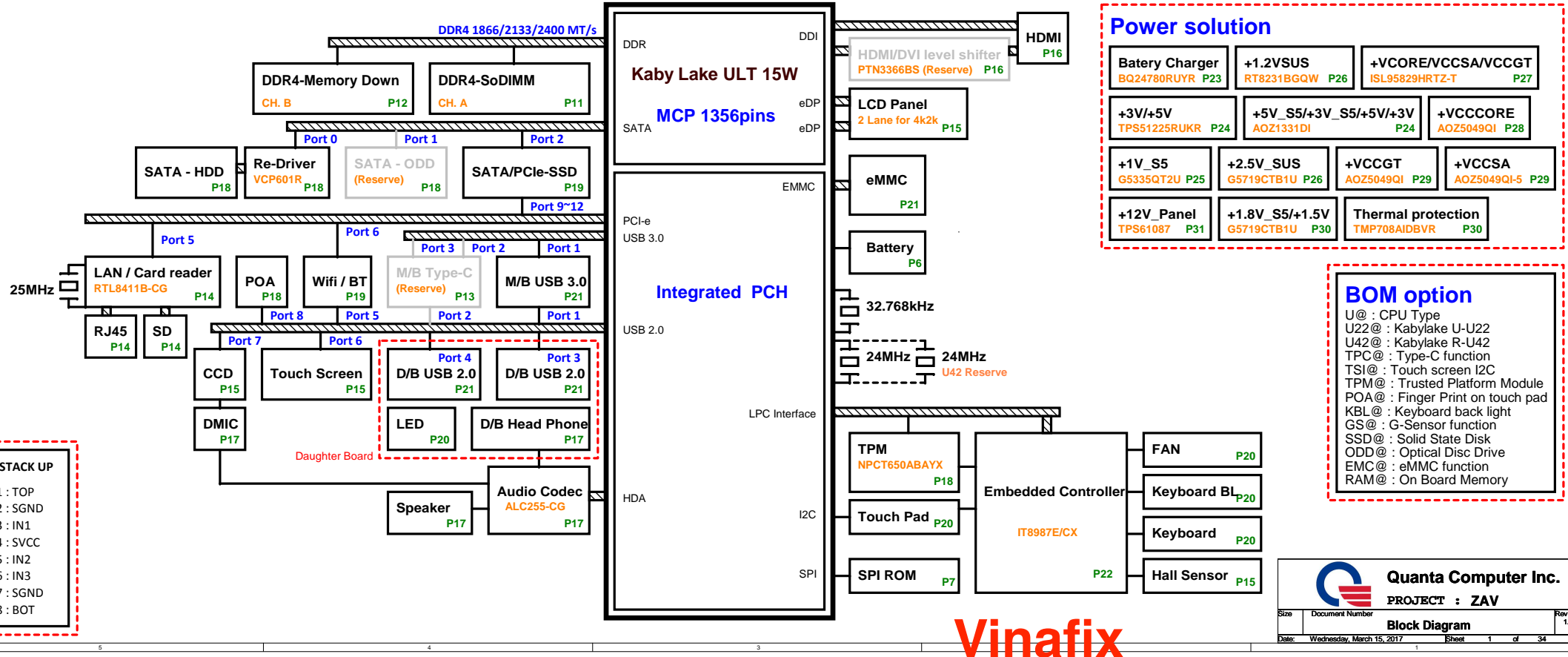
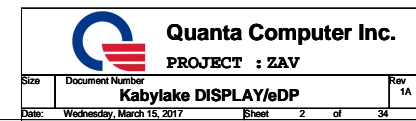


ZAV KabyLake-U/R series UMA Platform Block Diagram



Vinafix

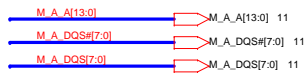


Change Data and DQS to interleave.

KabyLake ULT (DDR4)

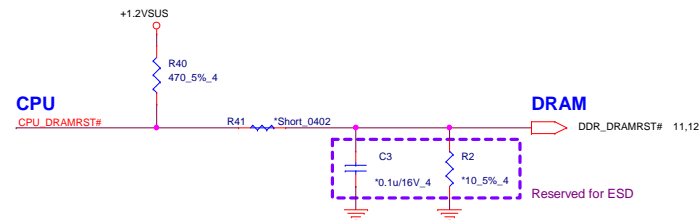


U@BGA1356P
2 OF 20

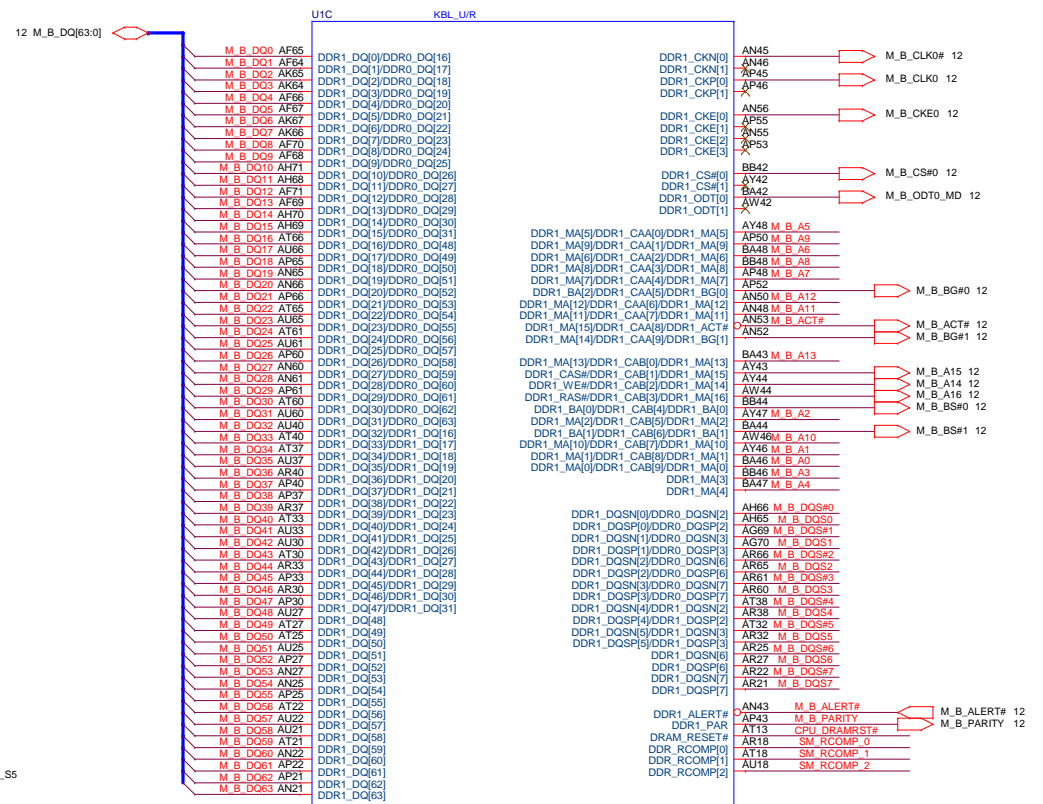
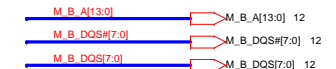


Stuff Q54 for both UMA and GPU in DDR_VTT_CNTL

DRAMRST



KabyLake ULT (DDR4)

U@BGA1356F
3 OF 20

DRAM COMP

**Quanta Computer Inc.**

PROJECT : ZAV

Size	Document Number	Rev
	Kabylake MEMORY	1A
Date:	Wednesday, March 15, 2017	Sheet 3 of 34

H_PECI (50ohm)
If route on microstrip,
Spacing need >18 mils
Trace Length: 2~15 inches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

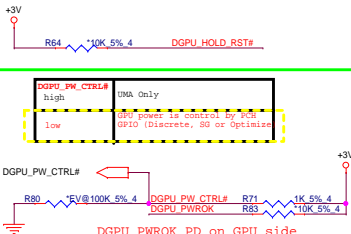


Touch PAD

Touch Screen

```
PU 2.2K for touch pad I2C bus(400 KHz)
```

GPU Control PU/PD



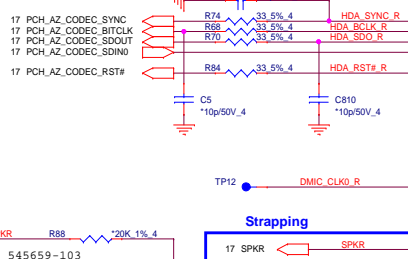
	DGPU_FW_CTRL#	VGA H/W Signal	Setup Menu	
UMA Only	1	UMA	Hidden	UMA boot
SG/Optimize	0	GPU	Hidden	GPU boot

UART2 for RMT

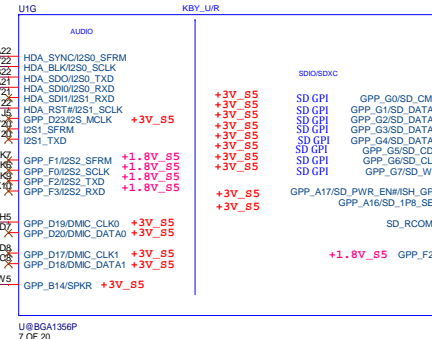
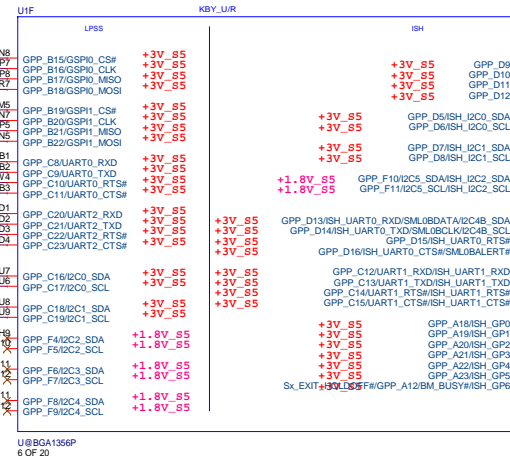
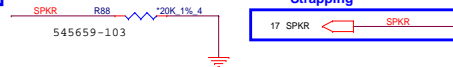
Touch PAD

Touch Screen

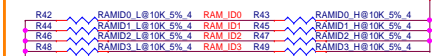
HDA



Strapping



RAM ID

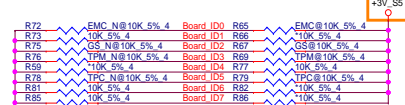


ID3	ID2	ID1	ID0	Vendor	Quanta PN
0	0	0	0	Hynix 8Gb	AKD5QG5TW05
0	0	0	1	Samsung 8Gb	AKD5QZ0T504
0	0	1	0	Micron 8Gb	AKD5QG5TL18
1	1	1	1	With out on board memory	

UART

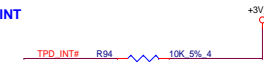


Board ID









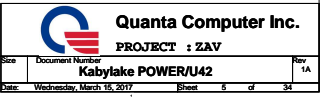
	Low	High
BOARD_ID0	Non eMMC	eMMC
BOARD_ID1	Reserved (Default)	Reserve
BOARD_ID2	Non G-sensor	G-sensor
BOARD_ID3	Non TPM	TPM
BOARD_ID4	Non Touch panel	Touch panel
BOARD_ID5	Non Type-C	Type-C
BOARD_ID6	Reserved (Default)	Reserve
BOARD_ID7	Reserved (Default)	Reserve

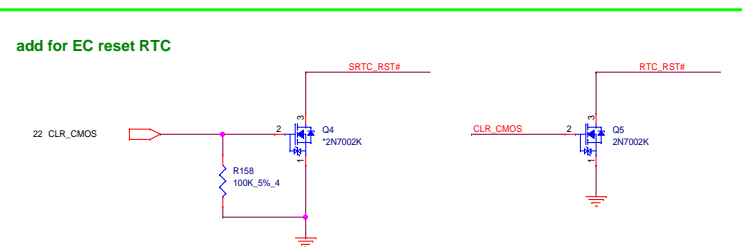
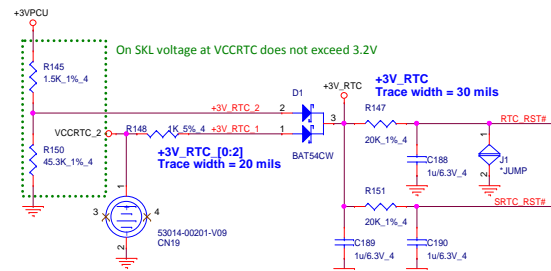
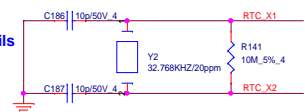
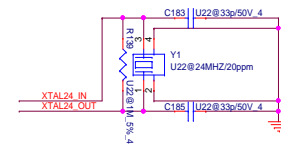
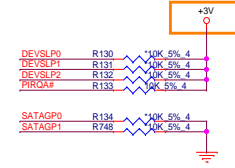
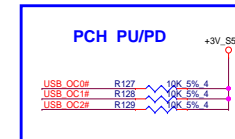
Touchpad INT

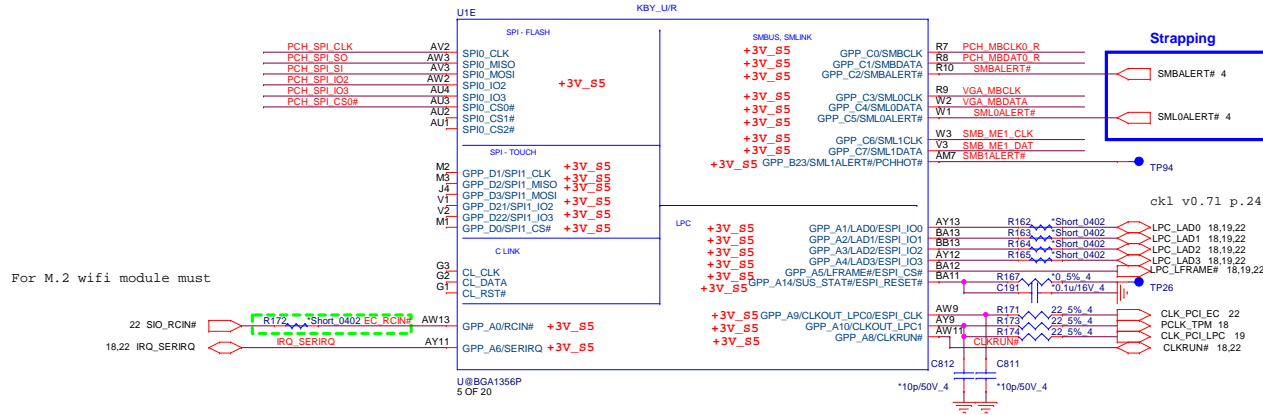


Skylake-U Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode	+3V 
GPP_B18 (GSPi0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V 
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Crypt to TLS(iPD 20K) 1 = Enable Intel ME Crypt to TLS	+3V_SS 
GPP_B22 (GSPi1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPi (iPD 20K) 1 = LPC	+3V 
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) 1 = eSPI selected for EC	+3V_SS 
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_I02	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_I03	Reserved	RSMRST#	(iPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal 
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) 1 =Port C is detected	

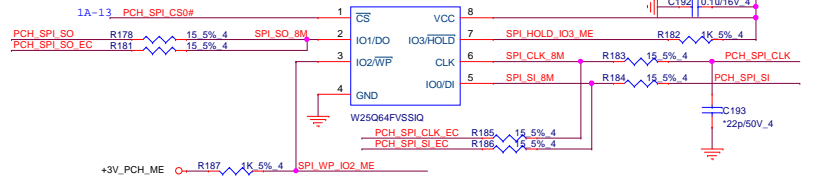






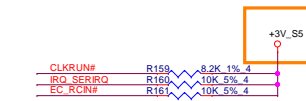
PCH SPI ROM(8M)
15ohm CS01502JB12
33ohm CS03302JB29

22 PCH_SPI_CLK_EC PCH_SPI_CLK_EC
22 PCH_SPI_SI_EC PCH_SPI_SI_EC
22 PCH_SPI_SO_EC PCH_SPI_SO_EC



SP@ socket P/N: DFHS08FS023 only for A-TEST

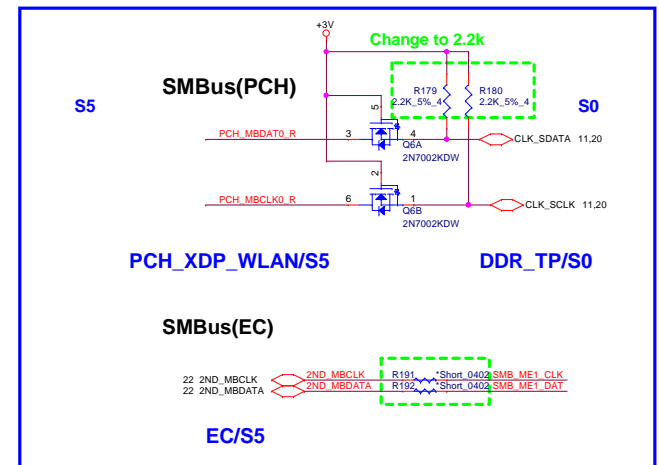
SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZN0Q00	GD25B64CSIGR
Kabylake 3.3V	WND	16M	AKE3DZN0N01	W25Q128FVSSIQ
	GGD	16M	AKE3DF00Q00	GD25B128CSIGR

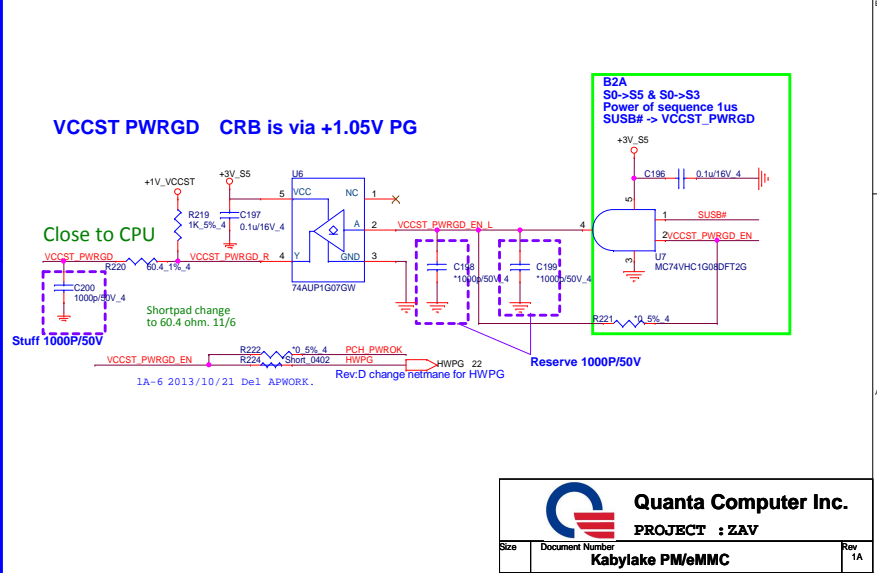
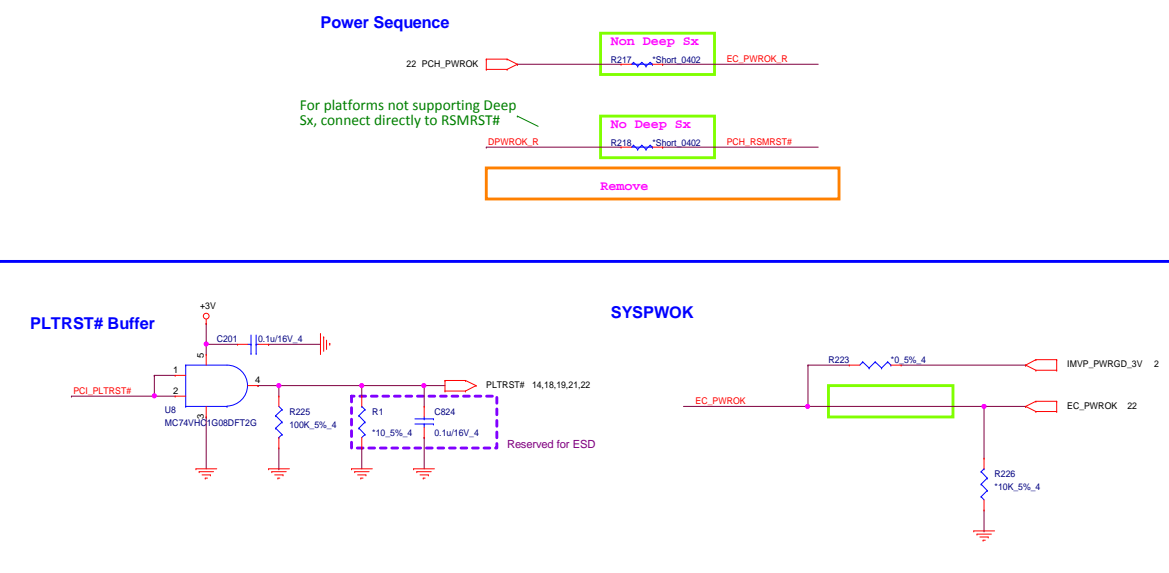
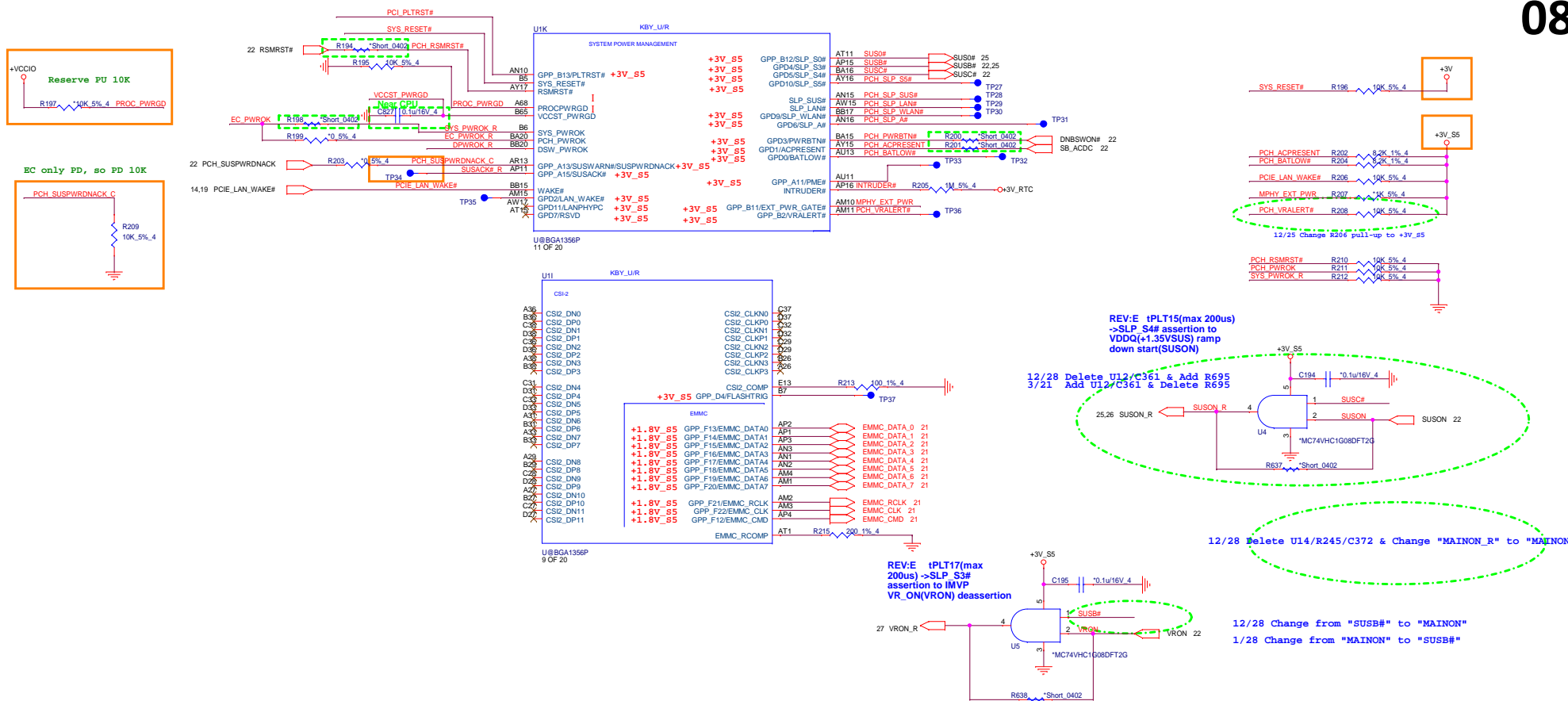


SMBus



Termination Resistor Requirement for PCH PCHHOT# Pin
Reserve PU 150K resistor

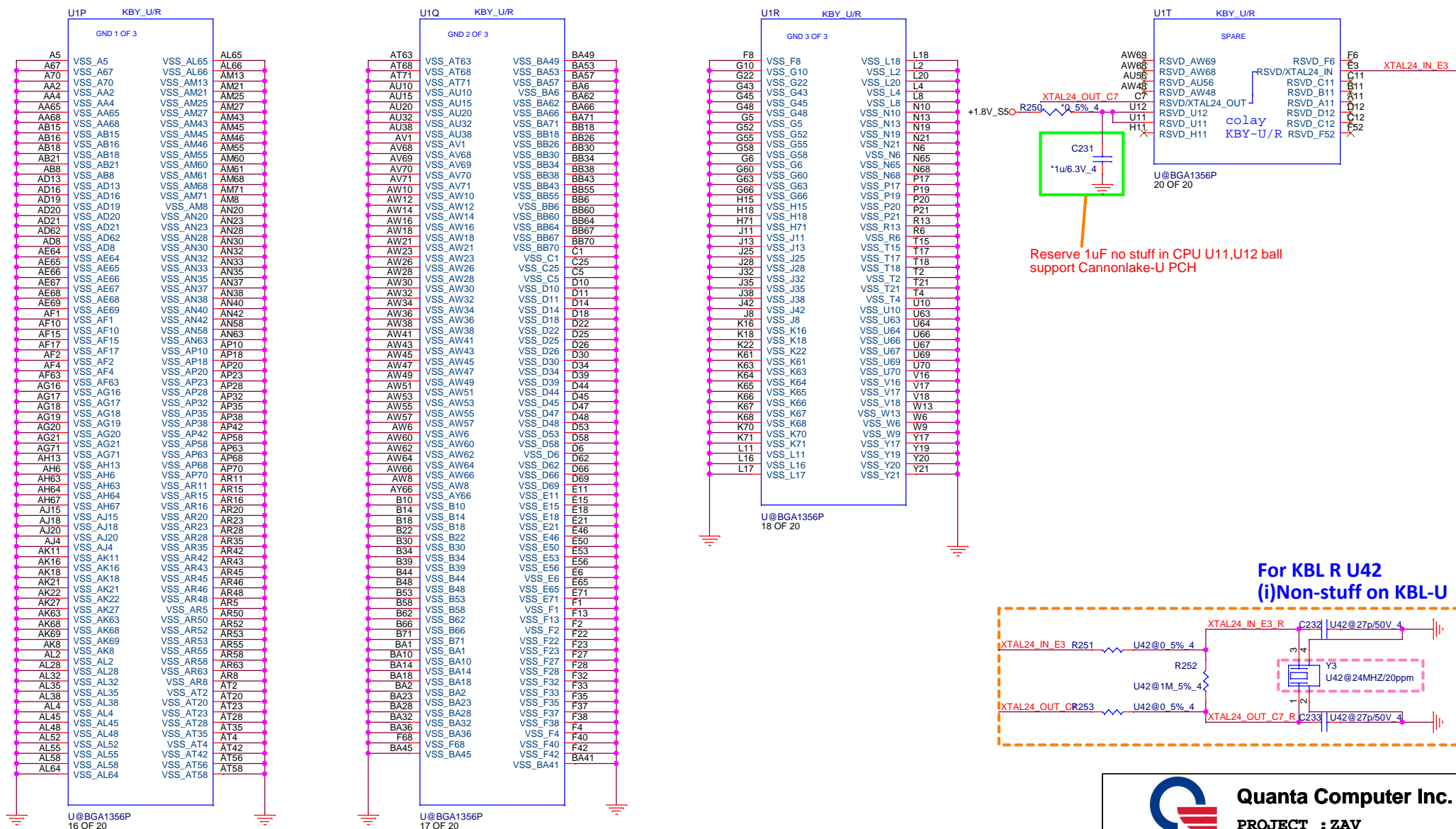


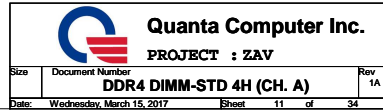




A

KabyLake ULT (GND)



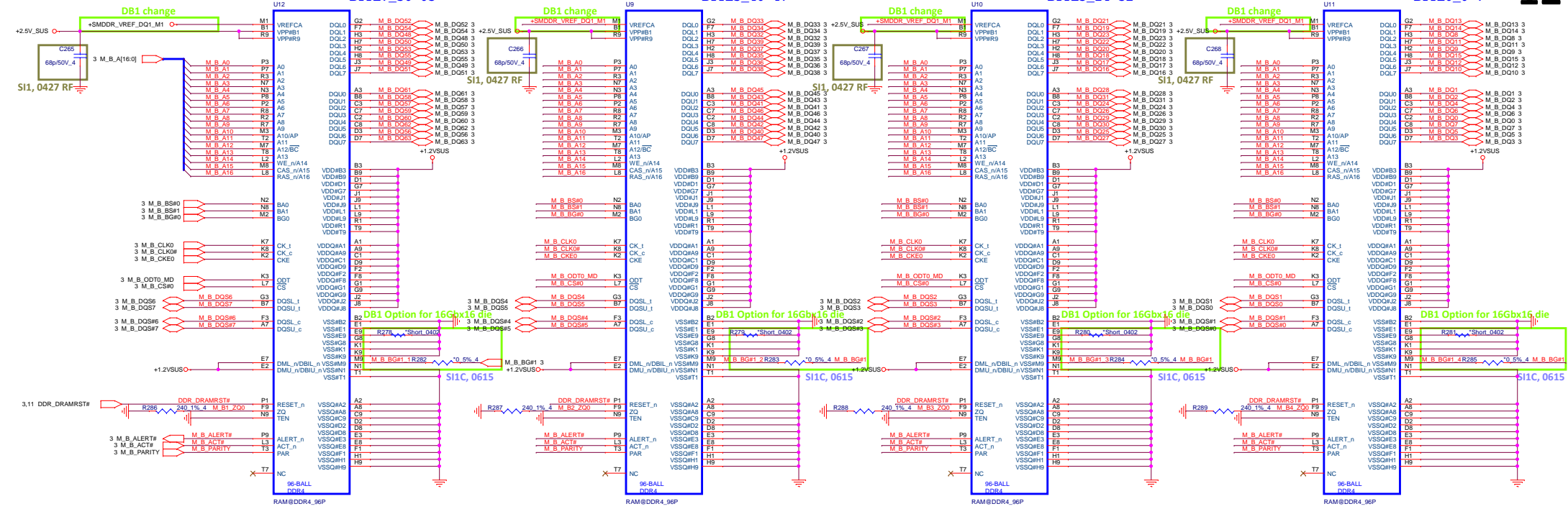


BYTE6_48-55
BYTE7_56-63

BYTE4_32-39
BYTE5_40-47

BYTE2_16-23
BYTE3_24-31

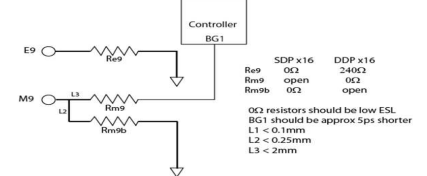
BYTE1_8-15
BYTE0_0-7



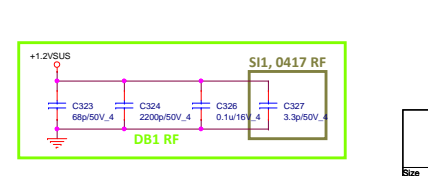
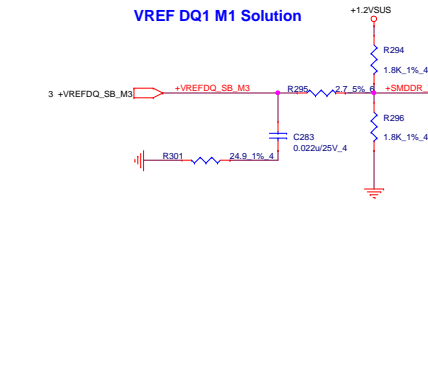
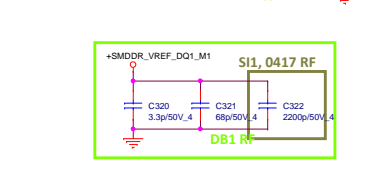
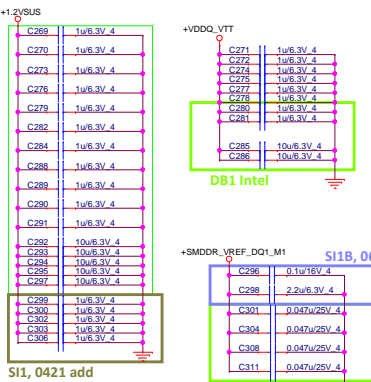
Vendor	P/N	Vendor	P/N
MIC 16G	AKD5G0TTL00	MT40A1G16HBA-083E1A	
Elpida			
SAMSUNG			



Memory 8G & Memory 16G TABLE	
Memory 8G	Memory 16G
R278 0Q CS000002JB38	240Q CS12402FB03
R279 0Q CS000002JB38	240Q CS12402FB03
R280 0Q CS000002JB38	240Q CS12402FB03
R281 0Q CS000002JB38	240Q CS12402FB03
R282 UNINSTAL	INSTAL
R283 UNINSTAL	INSTAL
R284 UNINSTAL	INSTAL
R285 UNINSTAL	INSTAL
R290 INSTAL	UNINSTAL
R291 INSTAL	UNINSTAL
R292 INSTAL	UNINSTAL
R293 INSTAL	UNINSTAL

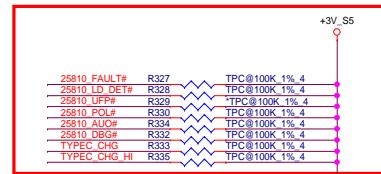


Place these Caps near Channel B
1uF/10uF 4pcs on each side of connector





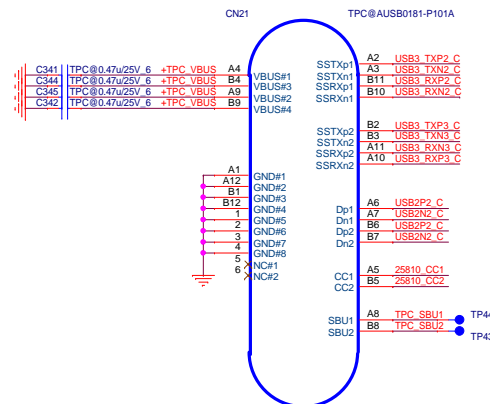
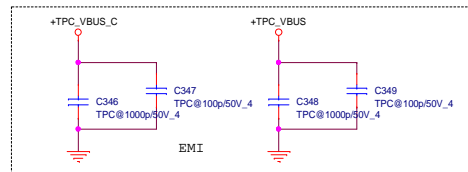
+5V_S!



25810_UFP# R341 *Short_0402 PCH_TypeC_UPFb# 2

25810_FAULT# R343 *Short_0402 USB_OC2# 6

The schematic diagram illustrates the TPC_VBUS circuit. A red wire, labeled +TPC_VBUS, carries the signal from the +TPC_VBUS input. This signal line is connected to two capacitors, C338 (100nF) and C339 (100pF), which are connected in parallel to ground. The output of this parallel combination is connected to the VBUS pin of the EC1 module (TPC@AZ5725-01F.R7G). The EC1 module is also connected to ground at pin 2.



U15

1 LINE-1 LINE-2 9 USB3 TXN2 C

2 LINE-3 LINE-4 8 USB3 RXP2 C

3 GND

4 USB3 TXN3 C

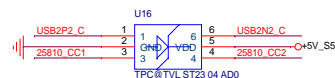
5 USB3 RXN3 C

6 USB3 TXP3 C

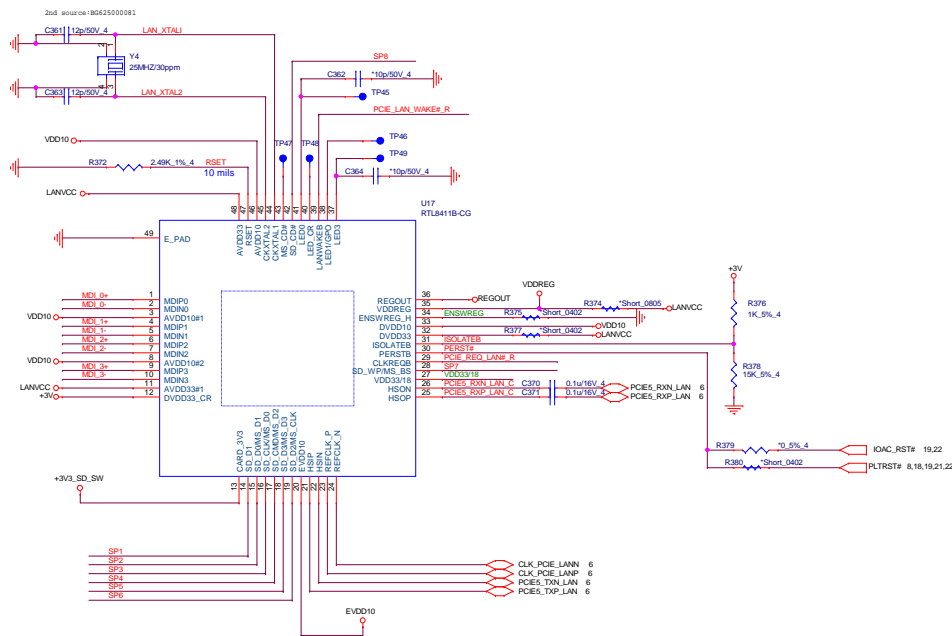
7 USB3 RXN3 C

8 USB3 TXN2 C

TPC@AZ1045-08F.R7G



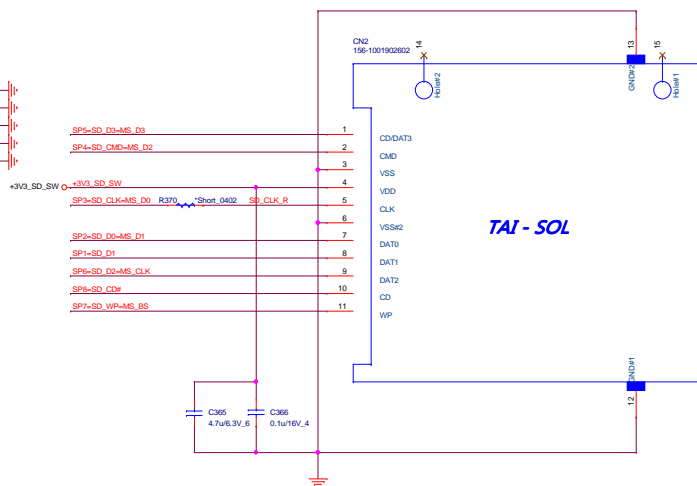
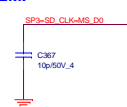
LAN & Card reader Combo (LAN)



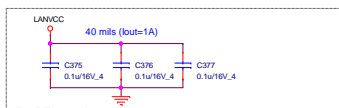
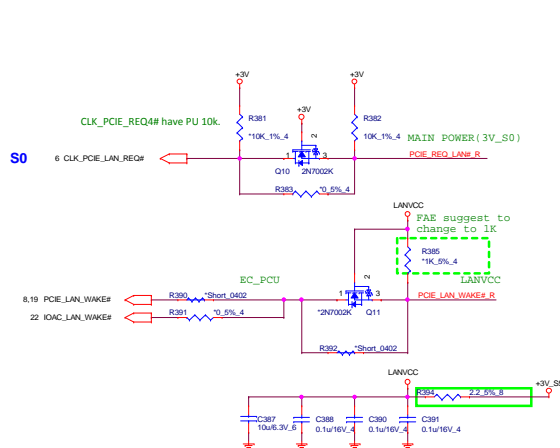
Card Reader (CRD)

SP1	R365	*Short_0,402	SP1-SD D1
SP2	R366	*Short_0,402	SP2-SD D0=MS D1
SP3	R367	*Short_0,402	SP3-SD CLK=MS D0
SP4	R364	*Short_0,402	SP4-SD CMD=MS D2
SP5	R368	*Short_0,402	SP5-SD D3=MS D3
SP6	R369	*Short_0,402	SP6-SD D2=MS CLK
SP7	R371	*Short_0,402	SP7-SD WP=MS BS
SP8	R373	*Short_0,402	SP8-SD CD#

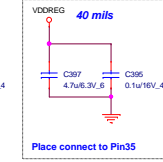
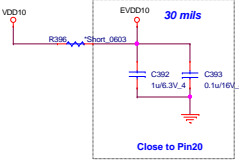
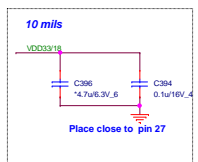
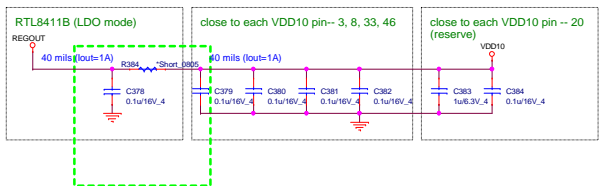
SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS RS
SP8	SD C0#	
SP9		MS INS#



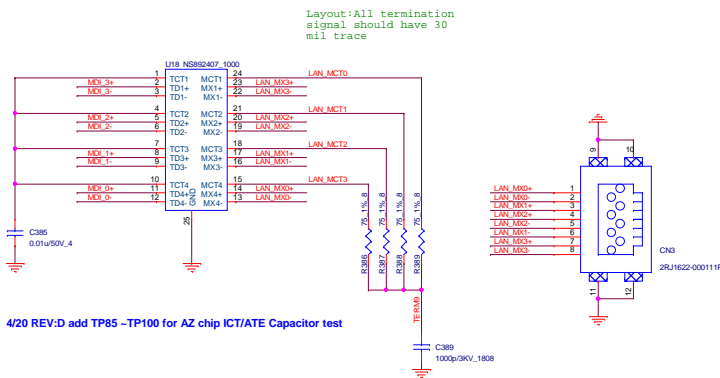
Leakage circuit (MPC)



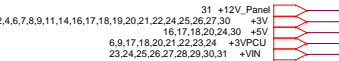
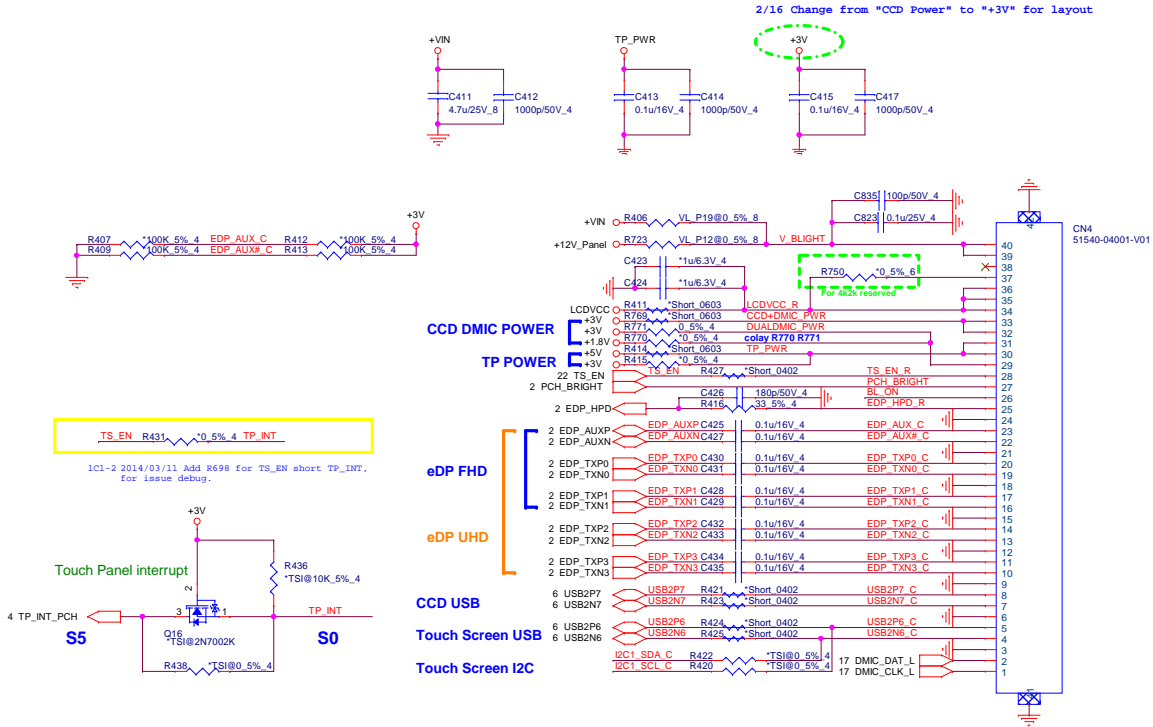
For RTL8411B
Place 0.1uF,CAP close to each VDD33 pin -- 11,32,48



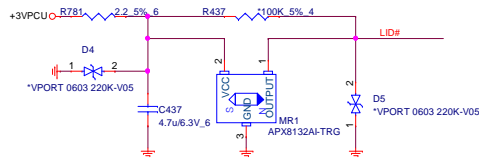
Transformer



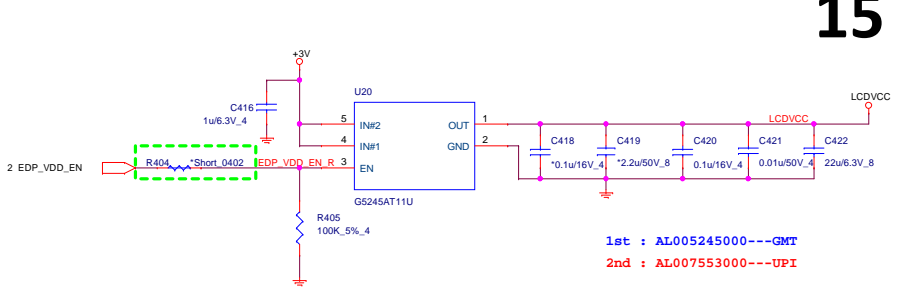
eDP/CCD



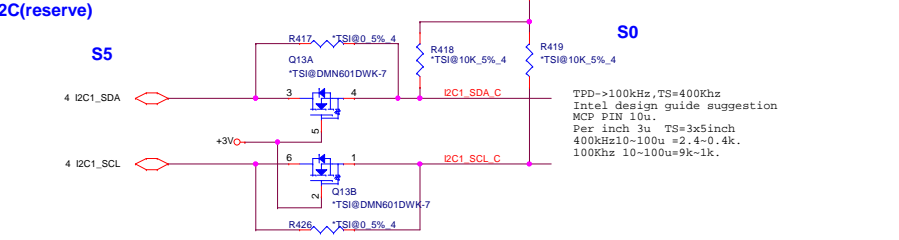
Hall Sensor (HSR)



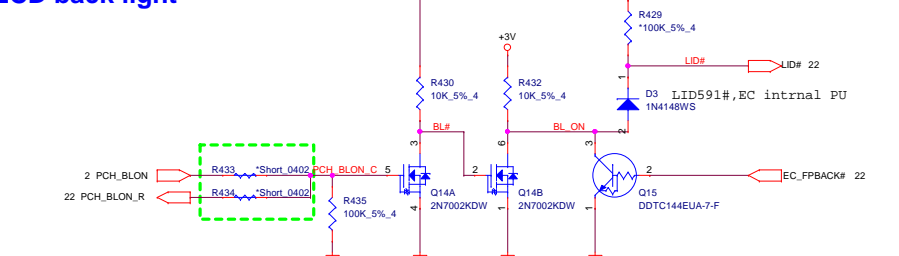
LCD Power



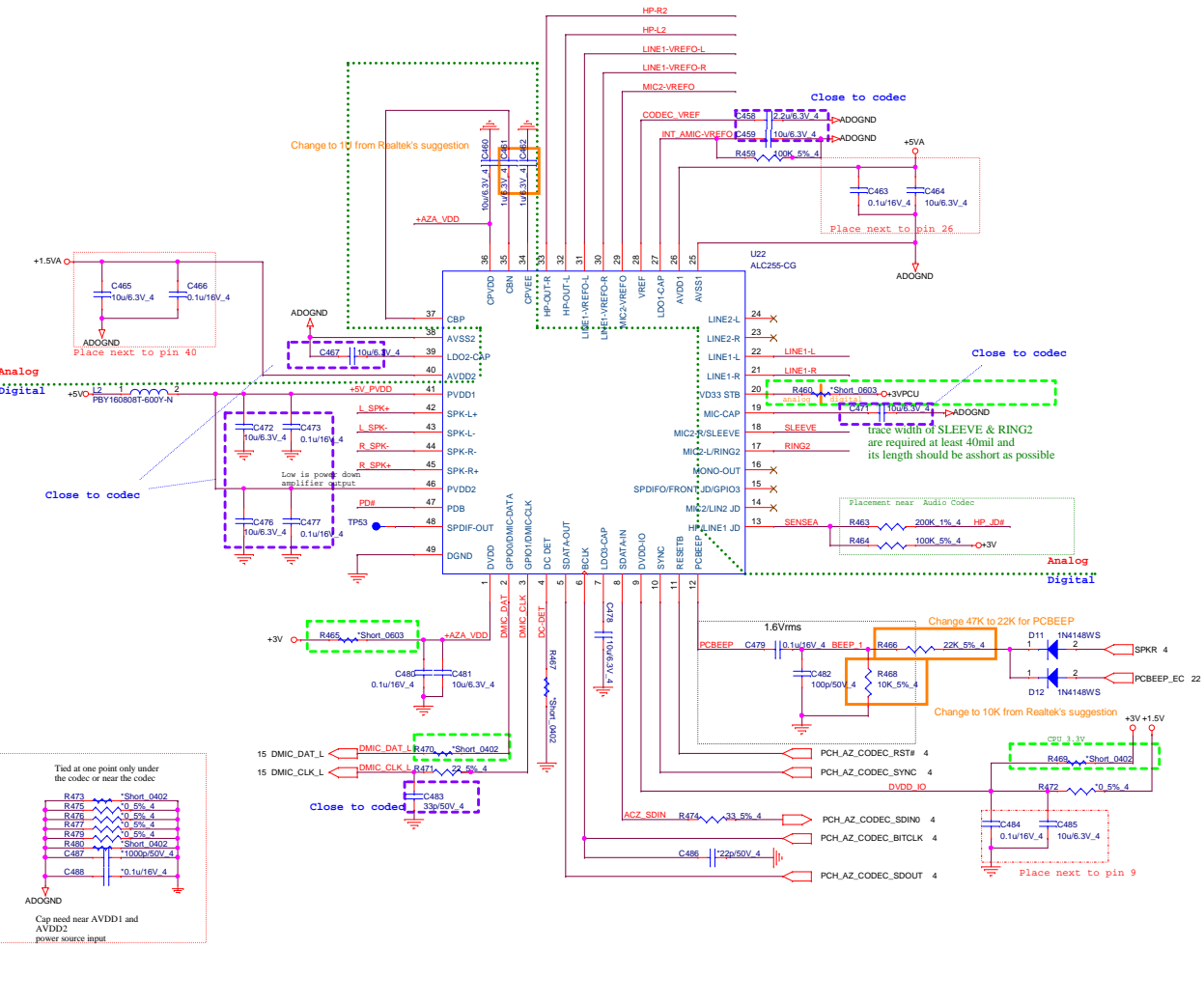
Touch screen level shift



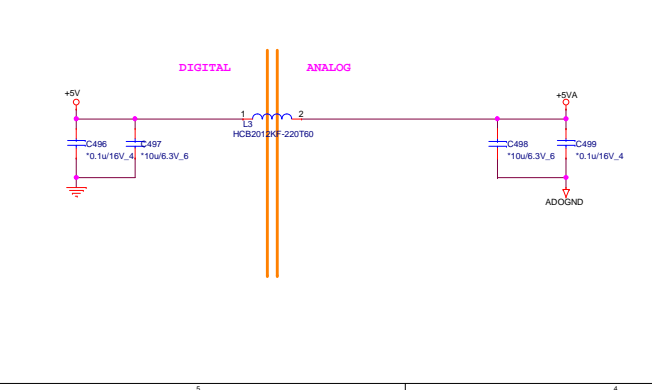
LCD back light



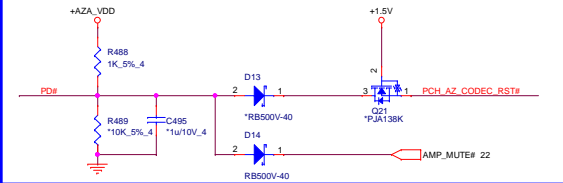
PROJECT : ZAV		
eDP/CCD/HS/TS		
Size	Document Number	Rev 1A
Date: Wednesday, March 15, 2017		
Sheet 15 of 34		



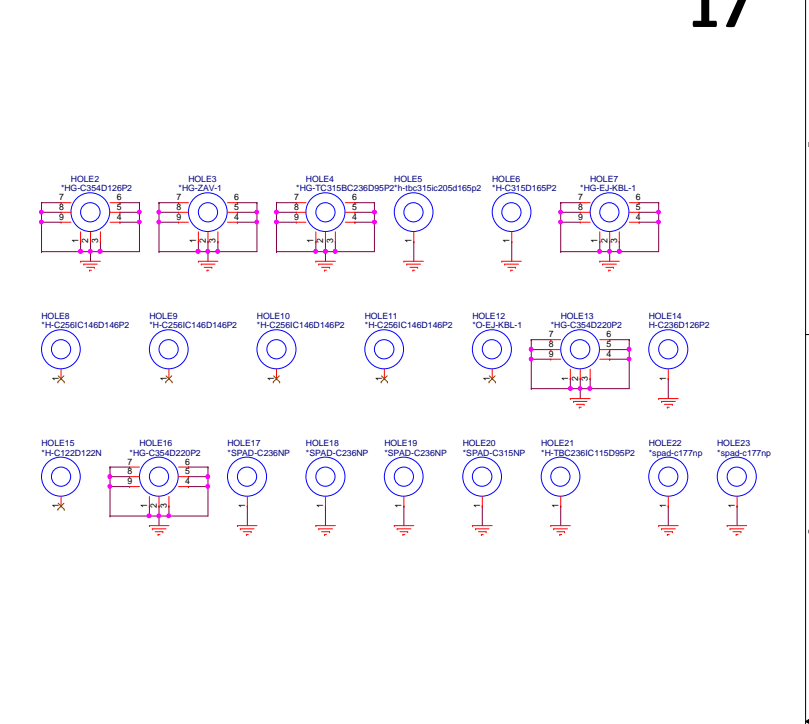
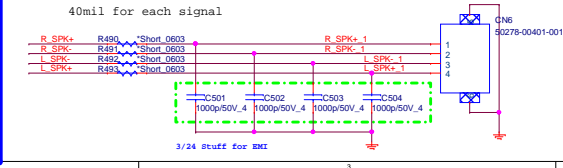
Codec PWR 5V(ADO)



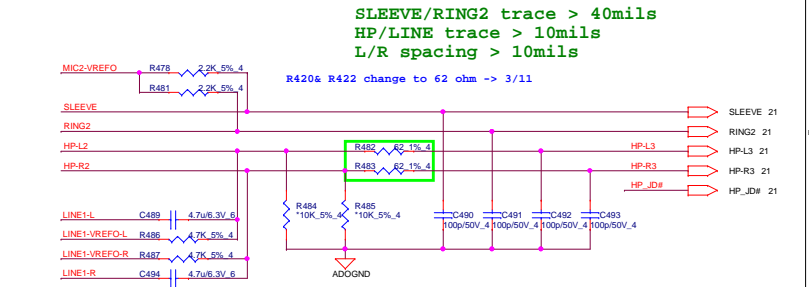
Mute(ADO)



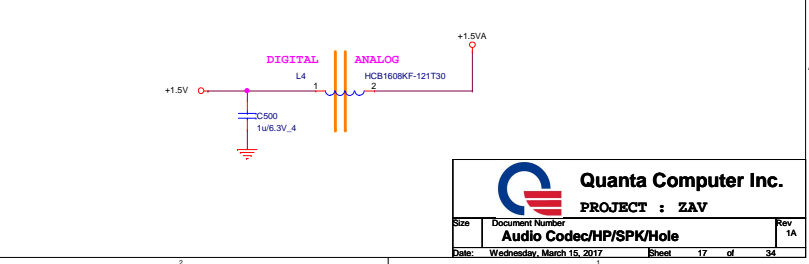
Internal Speaker



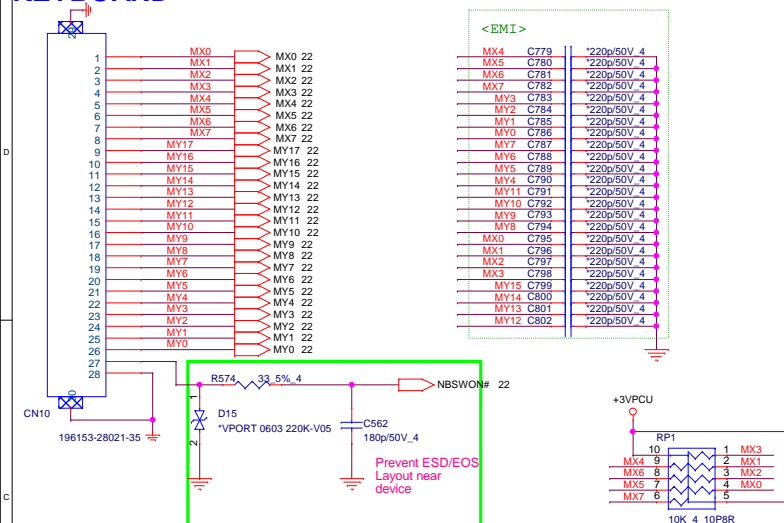
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



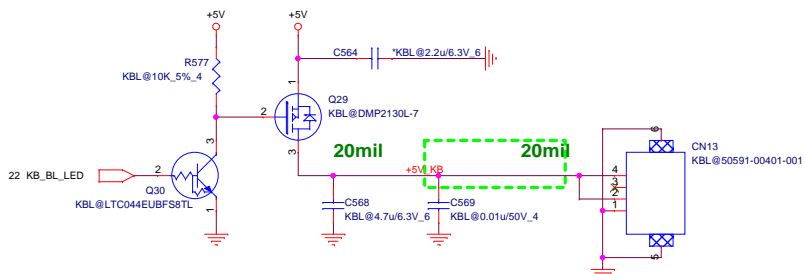
Codec PWR 1.5V(ADO)



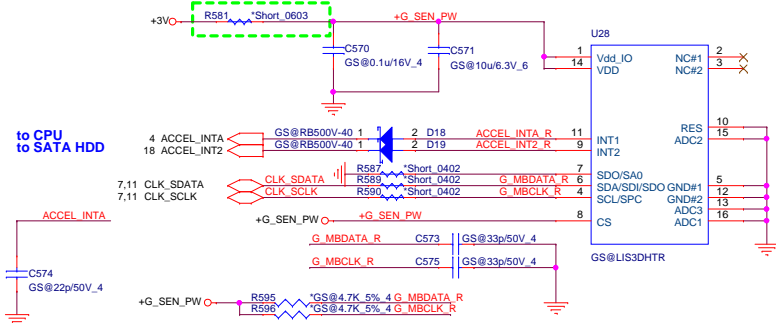
KEYBOARD



KB_BL LED (KBL@)

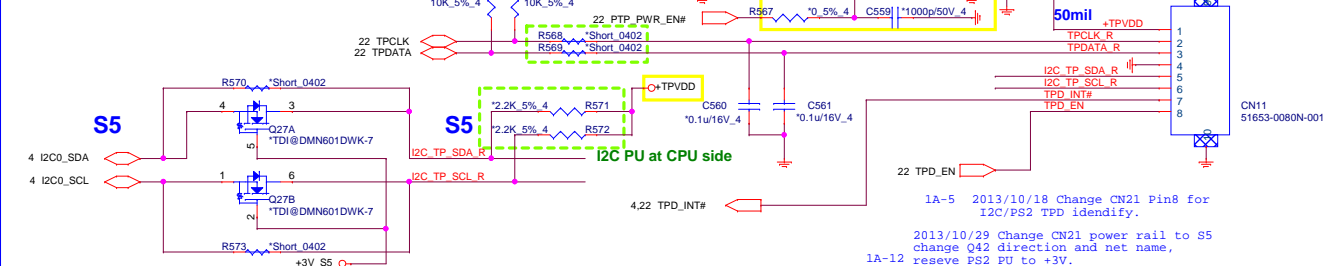


G-sensor (GS@)

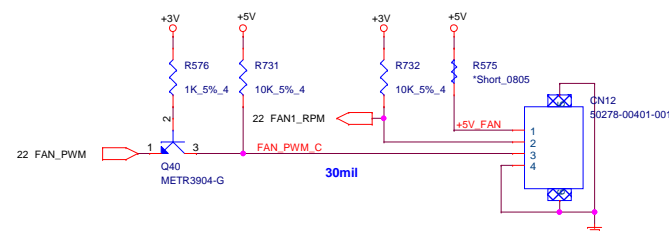


TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay) (TPD)

TPD->100KHz, TS=400KHz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400KHz 10-100u = 2.4-0.4k.
100KHz 10-100u=9k-1k.



CPU FAN (THM)



POWER LED (UIF)

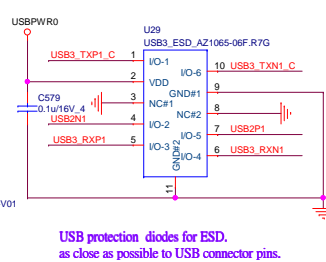
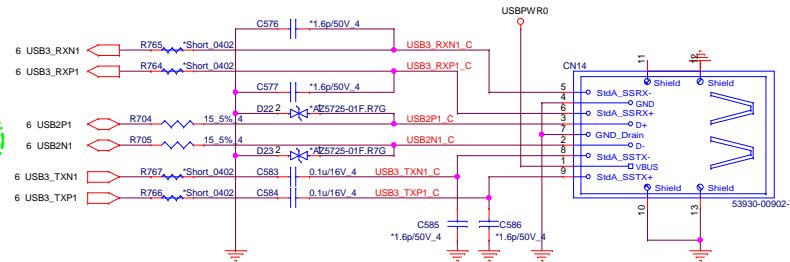
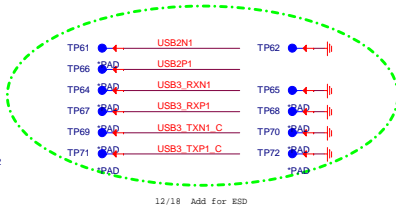
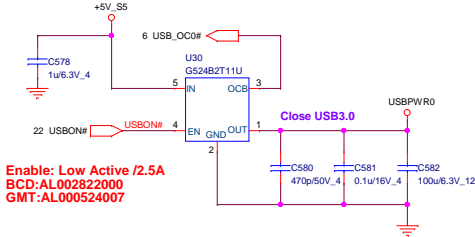
For EJ15 change to D/B



Quanta Computer Inc.
PROJECT : ZAV

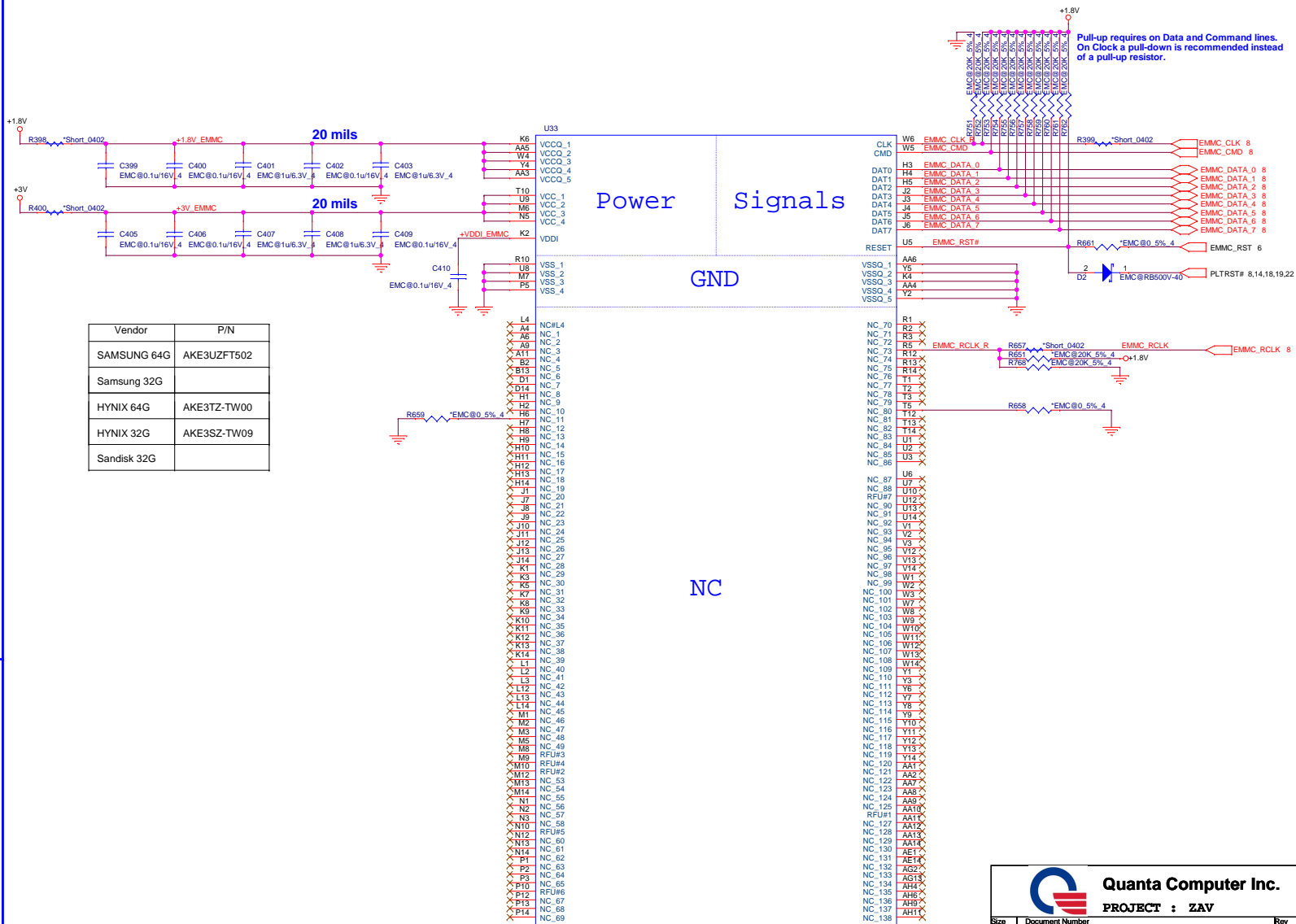
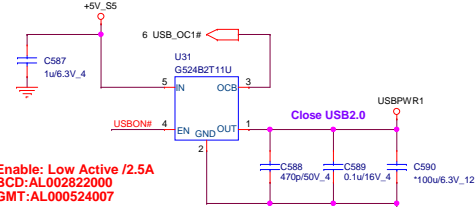
Size	Document Number	Rev
	KB/BL/TP/FAN/G-sensor	1A
Date:	Wednesday, March 15, 2017	Sheet 20 of 34

USB3.0 (MB/UB3)




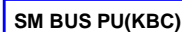
21

USB2.0 (DB/UB2)



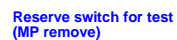
Vendor	P/N
SAMSUNG 64G	AKE3UZFT502
Samsung 32G	
HYNIX 64G	AKE3TZ-TW00
HYNIX 32G	AKE3SZ-TW09
Sandisk 32G	

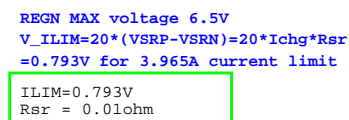
 Quanta Computer Inc. PROJECT : ZAV	
Size	Document Number
USB Port/eMMC/LED/DB	
Date:	Wednesday, March 15, 2017
Sheet	21 of 34



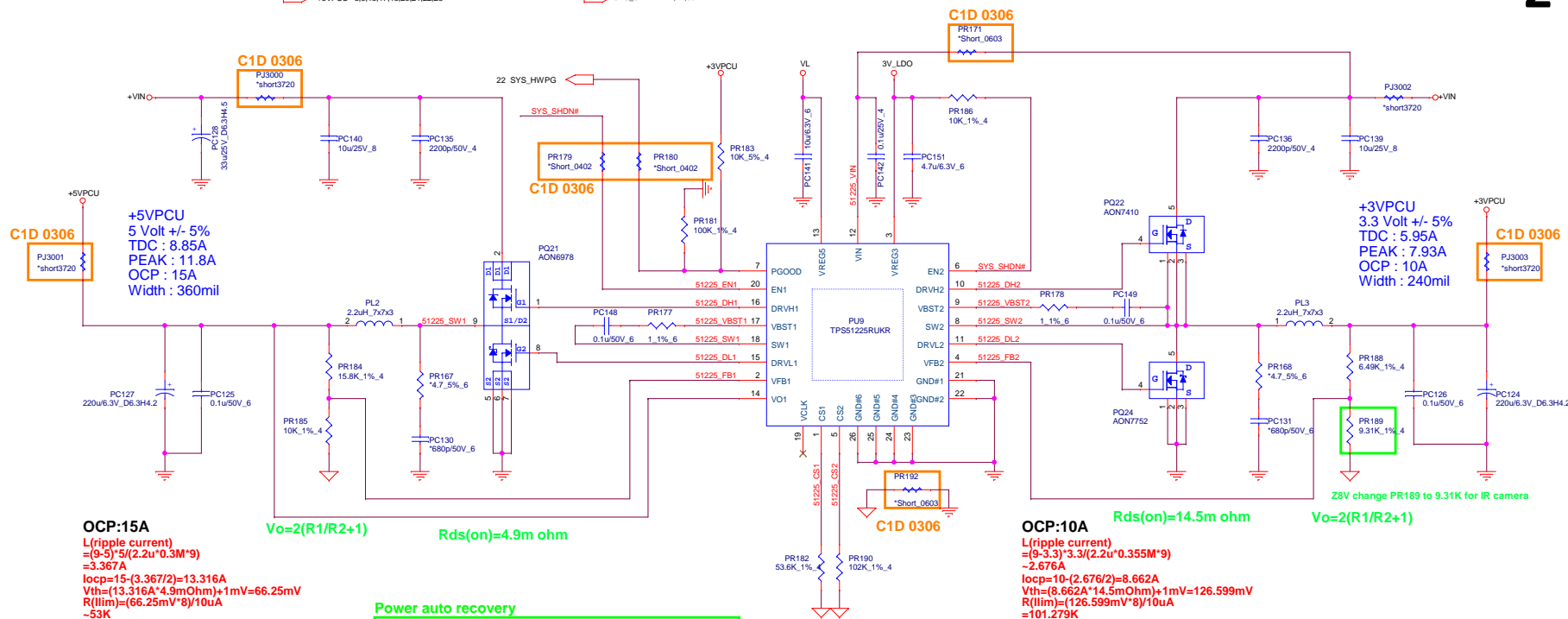
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

Reset SW (FSW)

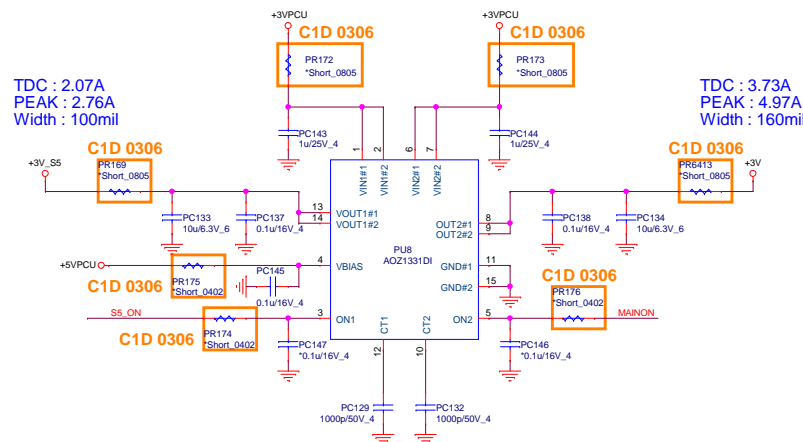
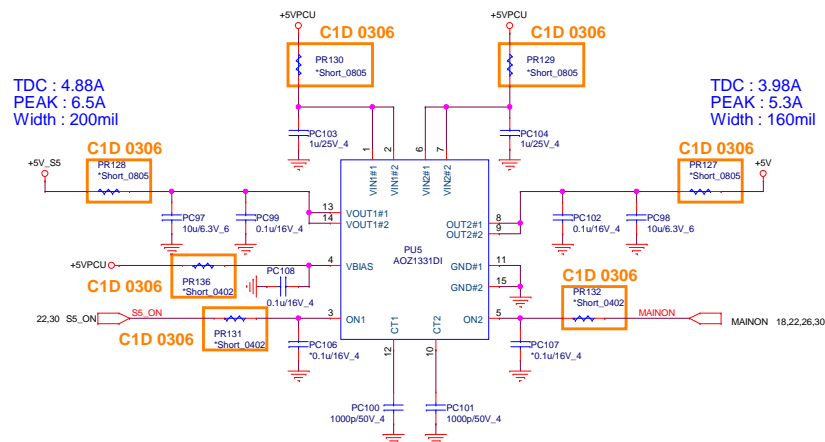


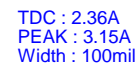
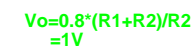


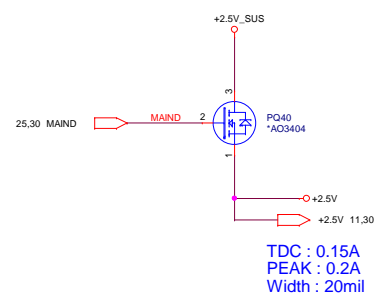
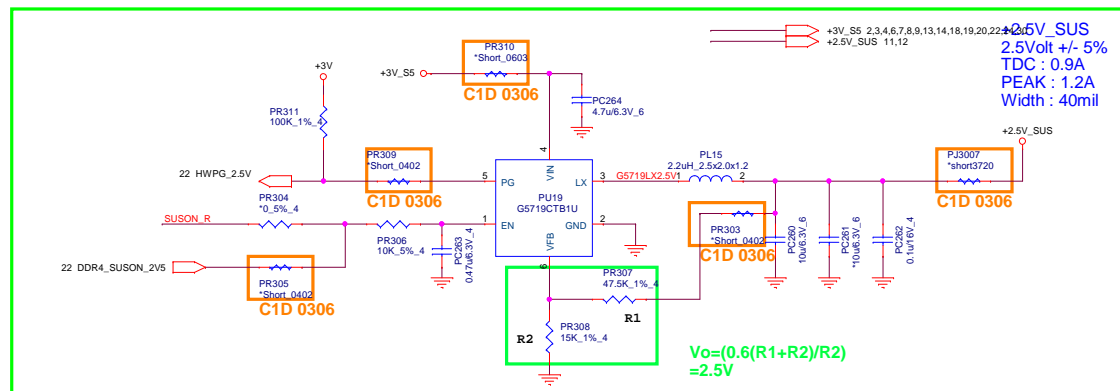
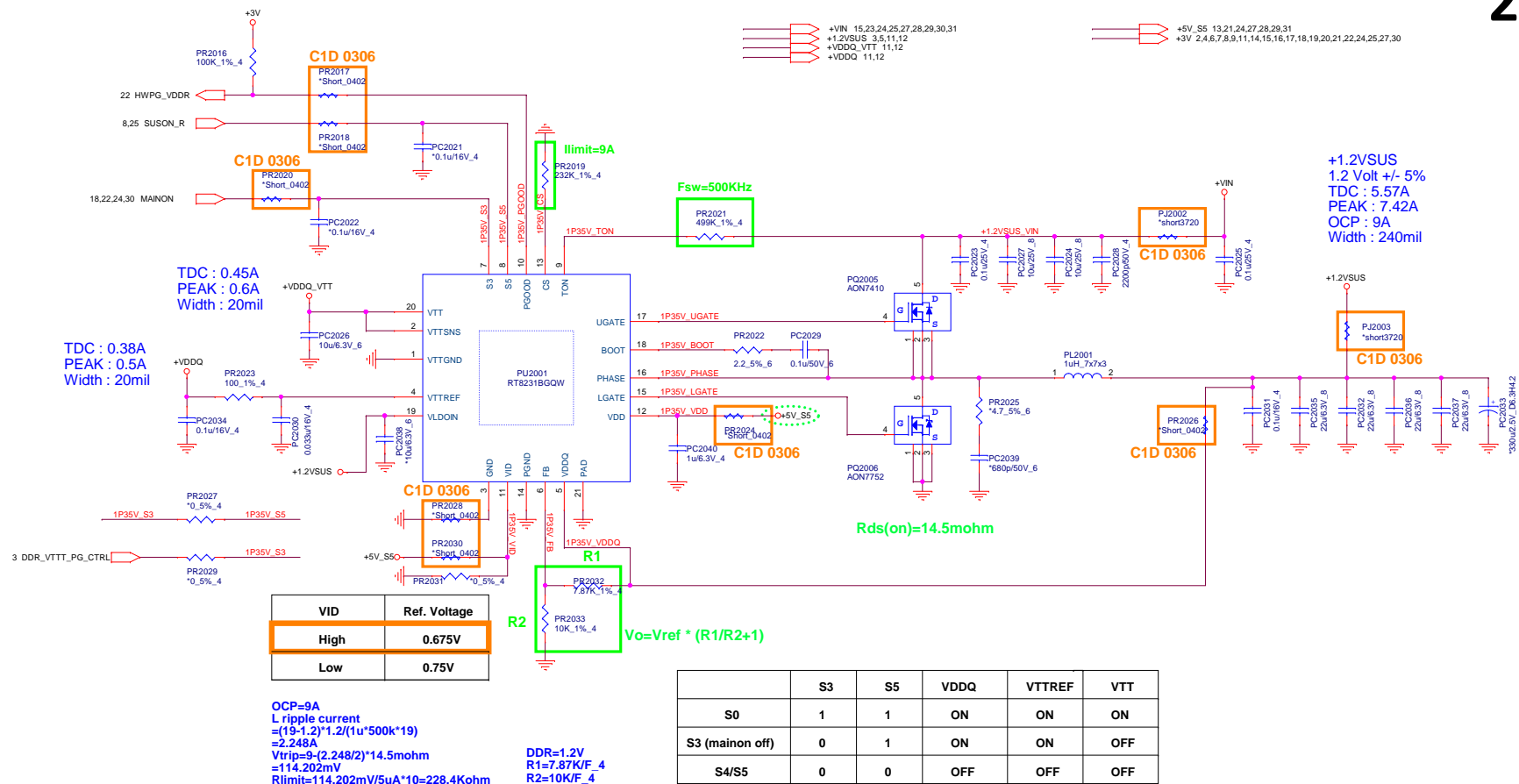
+VIN 15,23,25,26,27,28,29,30,31
+5VPCU 18,25
+3VPCU 6,8,15,17,18,20,21,22,23
VL 30
SYS_SHDN# 2,22,30



+5V_S5 13,21,26,27,28,29,31
+5V_S5 15,16,17,18,20,30
+3V_S5 2,3,4,6,7,8,9,13,14,18,19,20,22,26,30
+3V_S5 2,4,6,7,8,9,11,14,15,16,17,18,19,20,21,22,25,26,27,30

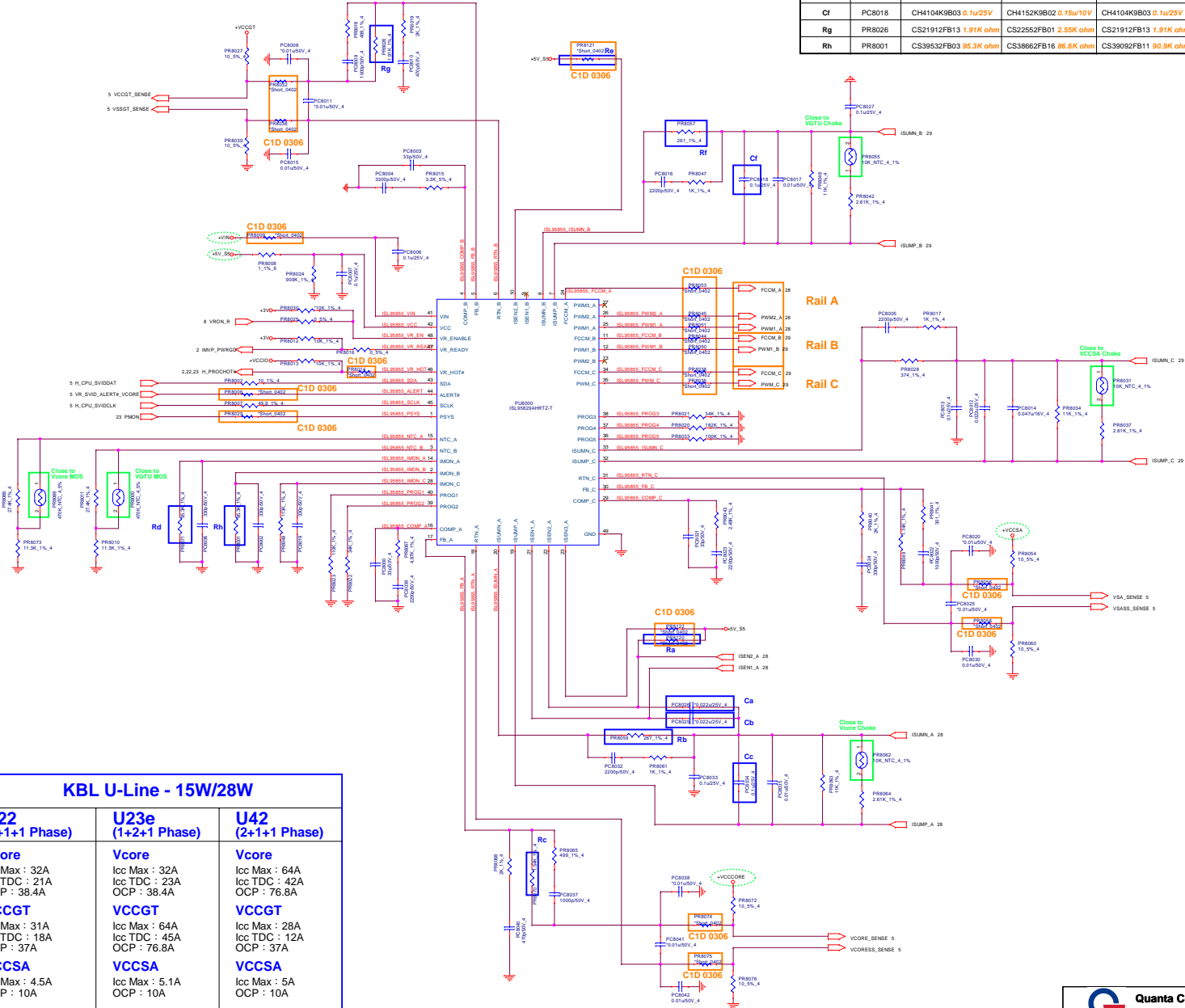
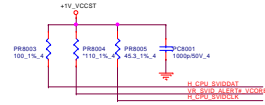






IMVP8 Vcore Controller

Rail A : Vcore
Rail B : VCCGT
Rail C : VCCSA




KBL U-Line - 15W/28W		
U22 (1+1+1 Phase)	U23e (1+2+1 Phase)	U42 (2+1+1 Phase)
Vcore Icc Max : 32A Icc TDC : 21A OCP : 38.4A	Vcore Icc Max : 32A Icc TDC : 23A OCP : 38.4A	Vcore Icc Max : 64A Icc TDC : 42A OCP : 76.8A
VCCGT Icc Max : 31A Icc TDC : 18A OCP : 37A	VCCGT Icc Max : 64A Icc TDC : 45A OCP : 76.8A	VCCGT Icc Max : 28A Icc TDC : 12A OCP : 37A
VCCSA Icc Max : 4.5A OCP : 10A	VCCSA Icc Max : 5.1A OCP : 10A	VCCSA Icc Max : 5A OCP : 10A

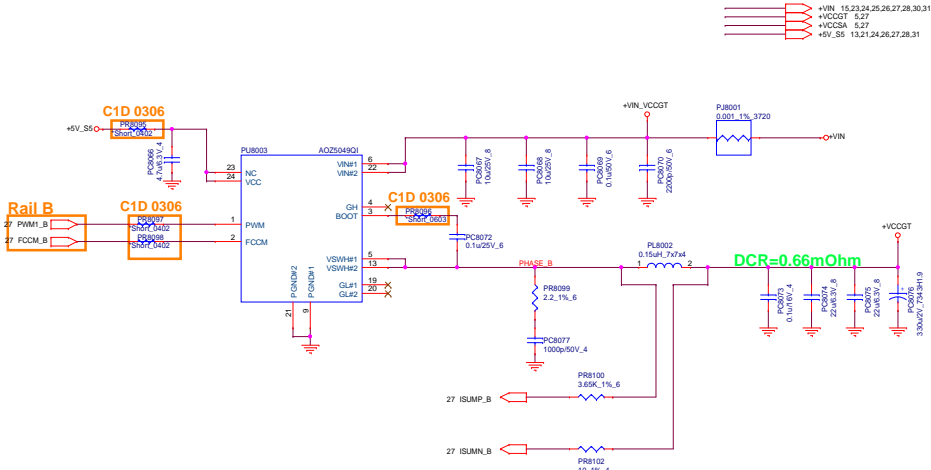
Item	Location	U22	U23e	U42
Ra	PR8120	CS00002JB38 0 ohm	CS00002JB38 0 ohm	Unstuff
Ca	PC8026	Unstuff	Unstuff	CH3224K1B01 0.022U/25V
Cb	PC8029	Unstuff	Unstuff	CH3224K1B01 0.022U/25V
Rb	PR8059	CS12672FB02 267 ohm	CS12672FB02 267 ohm	CS13322FB10 332 ohm
Cc	PC8034	CH4104K9B03 0.1u/25V	CH4104K9B03 0.1u/25V	CH4152K9B02 0.15u/10V
Rc	PR8070	CS21542FB00 1.54K ohm	CS21542FB00 1.54K ohm	CS23092FB00 3.09K ohm
Rd	PR8071	CS39532FB03 95.3K ohm	CS39312FB15 93.1K ohm	CS38662FB16 86.6K ohm
Re	PR8121	CS00002JB38 0 ohm	Unstuff	CS00002JB38 0 ohm
Cd	PC8028	N/A	CH3224K1B01 0.022U/25V	N/A
Ce	PC8031	N/A	CH3224K1B01 0.022U/25V	N/A
Rf	PR8067	CS12612FB13 261 ohm	CS13322FB10 332 ohm	CS12612FB13 261 ohm
Cf	PC8018	CH4104K9B03 0.1u/25V	CH4152K9B02 0.15u/10V	CH4104K9B03 0.1u/25V
Rg	PR8026	CS21912FB13 1.91K ohm	CS22552FB01 2.55K ohm	CS21912FB13 1.91K ohm
Rh	PR8001	CS39532FB03 95.3K ohm	CS38662FB16 86.6K ohm	CS39092FB11 90.9K ohm

27



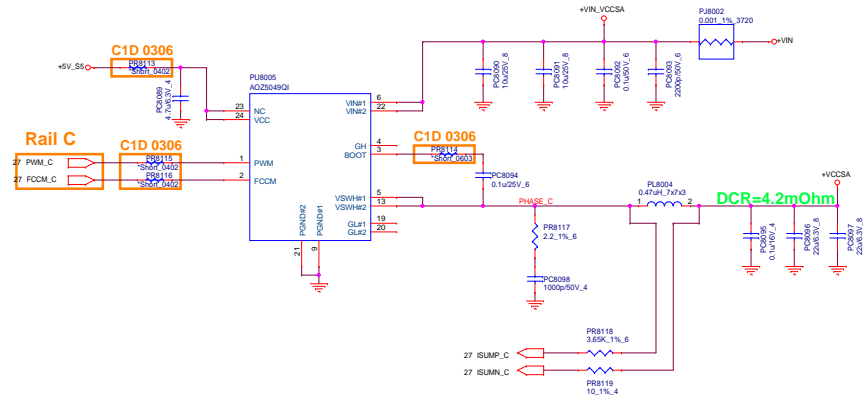
 Quanta Computer Inc. PROJECT : ZAV	
Size	Document Number VCCORE
Date:	Wednesday, March 15, 2017 Sheet 28 of 34 Rev 1A

VCCGT

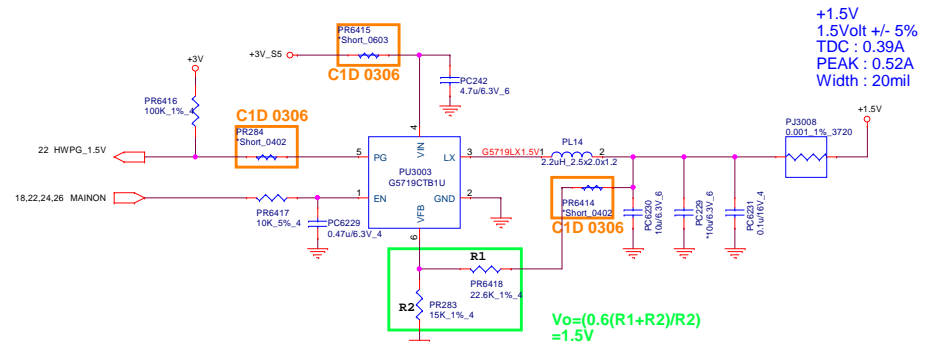
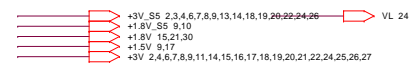
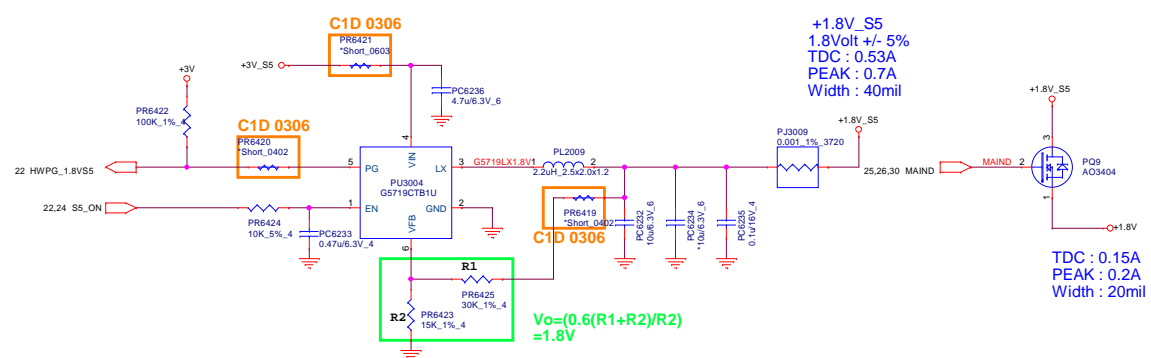


U22	U23e	U42
VCCGT	VCCGT	VCCGT
Icc Max : 31A	Icc Max : 64A	Icc Max : 28A
Icc TDC : 18A	Icc TDC : 45A	Icc TDC : 12A
OCP : 37A	OCP : 76.8A	OCP : 37A

VCCSA



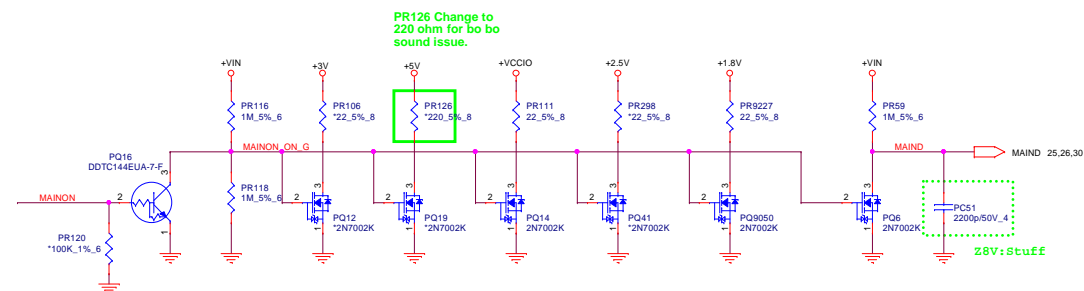
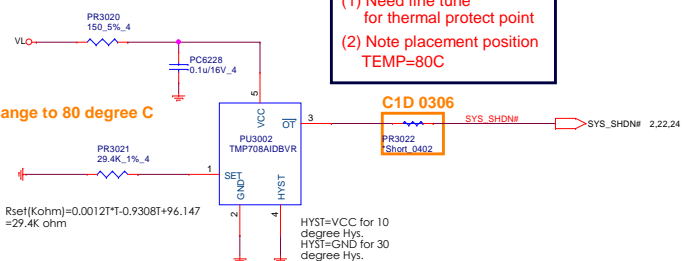
U22	U23e	U42
VCCSA	VCCSA	VCCSA
Icc Max : 4.5A	Icc Max : 5.1A	Icc Max : 5A
OCP : 10A	OCP : 10A	OCP : 10A



Thermal protection

- (1) Need fine tune for thermal protect point
- (2) Note placement position TEMP=80C

Thermal request change to 80 degree C



Model	Date	Change List
ZAV Rev. A A-stage	11/07	1. FIRST RELEASED 2. Remove all the GT3e part. 3. Change the eDP connector pindefine. (page 15) 4. Add all the function part BOM option. 5. Reserve 0 ohm resistor R704, R705 for USB 2.0 port2. (page 21)
	11/08	1. Add colay circuit on HDMI. (page 16) 2. Remove Type-C re-driver circuit. (page 13)
	11/09	1. Change EC pin97 for VLED enable control pin. (page 15, 22) 2. Change the FAN block from 3-pin to 4-pin circuit. (page 20) 3. VLED +12V circuit change to power part. (page 31)
	11/10	1. Swap FAN connector. (page 20) 2. Add ODD function. (page 18) 3. Remove DC-DET circuit. (page 17) 4. Change ODD power capacitor C740 size from 3528 to 1206. (page 18) 5. Change memory down Rx resistor frome 34.8±1% to 36±1% ohm. (page 12) 6. Change PJ2 part number to DFHD04MR237. (page 23) 7. Follow HSIO change the USB2.0 net name (page 6, 13, 15, 18, 19, 21)
	11/14	1. Reserve 0 ohm R750 for 4K2K panel. (page 15) 2. Add R751~R762 20k ohm for pull-up required on Data and Command lines. (page 21) 3. Change FFC connector from 30-pin to 34-pin for the future 17" case. (page 21.) 4. Reserved R764~R767 0 ohm for Tx Rx signle. (page 21)
	11/15	1. Add Hole 1~18. (page 17) 2. Modify PJ2 DC-IN connector. (page 23) 3. Reserve C810, C811 and C812 for EMI solution. (page 4, 7)
	11/16	1. Swap CN12 "PWM" pin-3 and "GND" pin-4. (page 20)
	11/17	1. Add R651, R768 20k ohm for pull-up required on Data and Command lines. (page 21) 2. Change Type-C USB2.0 ESD TVS package from DFN2510 to SOT23-6. (page 13) 3. Add R769 0 ohm for CCD and DMIC power supply. (page 15) 4. Change PJ2 part number and foot print. (page 23)
	11/18	1. Modify ODD pindefine and delete SSD_ID pin. (page 6, 18) 2. Add C813 3300pF for DDR4 memory down clock. (page 12) 3. Swap DDR4 memory channel A and B data line for layout house placement. (page 11, 12)
	11/22	1. Swap POA connector for placement. (page 18) 2. Charge 0.01uF part numer from CH3103K1B15 to CH31006KB18. (page 12, 18) 3. Charge 0.01uF part numer from CH3104J1B00 to CH31006KB18. (page 12, 18)
	11/23	1. Add C814 for HDD redriver IC power supply. (page 18) 2. Change R463 200k resistor error value 5% to 1%. (page 17) 3. Reserve R770, R771 for dual-DMIC power supply 3.3V and 1.8V. (page 15) 4. Reserve C815 ~ C822 22uF 6.3V for +VCCCORE. (page 5) 5. Change C44, C46, C48, C49, C50, C51, C53, C59, C60, C61, C62 from 1uF to 10uF. (page 5) 6. Change R109, R110, R115, R116, R117, R118 from 0_0805 ohm to 0.0002_0805 ohm. (page 5)
	11/24	1. Change PC2030 part number from to CH3473K1B00. (page 26) 2. Change PC232, PC8014 part number to CH3473K1B00. (page 25, 27) 3. Change PC8050, PC8073, PC8095, PC8061, PC6228 part number to CH4103K1B08. (page 23~31) 4. Change PC8051, PC8052, PC8074, PC8075, PC8096, PC8097, PC8062, PC8063 part number to CH6221M9A00. (page 23~31) 5. Swap Touch pad connector for placement. (page 20) 6. Swap DDR SODIMM for placement. (page 11) 7. Swap SSD connector. (page 19) 8. Modify HDMI colay circuit for routing guidelines. (page 16)
	11/25	1. Reserve R1, R2, C823,C824, C825 for simple ESD solution. (page 3, 8) 2. Update Hole. (page 17) 3. Change PC8024 and PC8040 from 30p_25V to 330p_50V. (page 27)
	11/28	1. Change R37 from 120 ohm to 200 ohm for SDP setting. (page 3) 2. Swap HDD connector for match Z8V's cable. (page 18) 3. Delete PQ28. (page 23)
	11/29	1. Keep PR23 value for the project ZAV. (page 23)
	11/30	1. Add full description and function code. (ALL) 2. Change HOLE footprint. (page 17) 3. Swap U12 DQ pin for placement. (page 12) 4. Swap U15 pin-5 and pin-6 for placement. (page 13)
	12/01	1. Change all the test point footprint from TP2075 to TP2050. (ALL)
ZAV Rev. B B-stage	12/14	1. Change U16 power supply from +TPC_VBUS to +5V_S5. (page 13)
	12/15	1. Change ODD connector from 14-pin to 18-pin. (page 18) 2. Stuff R152 for future dis. project used. (page 6) 3. Change CN19 RTC connector form cable type to socket type. (page 6) 4. Delete net 3V_LDO. (page 24) 5. Nunstuff PC228. (page 25) 6. Add Power tree. (page 34)
	12/19	1. Add R59 for Board_ID4 pull-low resistor. (page 4)
	12/20	1. Stuff C236 for ESD injection. (page 11) 2. Add C826,C827,C828,C829,C830,C831,C832,C833 for ESD injection. (page 6,8,9,22)
	12/21	1. Delete net DMIC_DATA0_R. (page 4) 2. Change CN21 part number from DFHS09FR365 to DFHS09FR758. (page 21)
	12/22	1. Change R411 size from 0805 to 0603. (page 15) 2. Change CN7 part number from DFHS20FS123 to DFHS20FS095. (page 18) 3. Change CN11 part number from DFFC08FR139 to DFFC08FR120. (page 20)

Model	Date	CHANGE LIST
ZAV Rev. B B-stage	12/23	1. Change CN7 footprint from gs12201-1011-9h-20p-l-smt to gs12201-1011-9h-20p-l. (page 18) 2. Change CN1 footprint from 51605-01801-001-18p-l to 132f18-100000-a2-r-1p-l. (page 18) 3. Change PJ3002 to short pad. (page 24)
	12/27	1. Modify HDMI co-layout circuit without PTN3366BS. (page 16)
	12/28	1. Change HOLE3 foot print to HG-ZAV-1. (page 17) 2. Change HOLE8, 9, 10, 11 foot print to H-IC146BC264D146PB. (page 17) 3. Change C183, C185 capacitor from 10pF to 27pF for frequency tolerance stability. (page 6) 4. Change C361, C363 capacitor from 10pF to 12pF for frequency tolerance stability. (page 14) 5. Change HOLE6 foot print to h-tbc315ic205d165p2. (page 17) 6. Add HOLE22, 23. (page17)
	12/29	1. Change Q26, Q29, Q34 part number from BAM34130001 to BAM21300000 for size and cost problem. (page 18,20) 2. Modify power part block diagram. (page 23~31)
	01/03	1. Change PC8012 to 0.022uF as per FAE's suggestion. (page 27) 2. Change PR8028 to 374ohm as per FAE's suggestion. (page 27) 3. Change PC8010, PC8040 to 470pF as per FAE's suggestion. (page 27) 4. Change PR8001, PR8071 to 95.3k ohm as per FAE's suggestion. (page 27)
ZAV Rev. C C-stage	01/10	1. Add U35, U36, D8, D9 for HDMI ESD solution. (page 16) 2. Change C206 0805_47uF to 0603_22uF. (page 9) 3. Add C834 0603_22uF. (page 9)
	01/11	1. Change type-c CN21 footprint to ub31-ausb0181-p101a-24p. (page 13) 2. Remove C825 for ESD solution C3 and R2. (page 3)
	01/13	1. Change CN3 foot print to rj45-jm361c-hp34aa03-9h-8p-smt for SMT P/R. (page 14)
	01/20	1. Change CN21 symbol to dummy block for layout placement. (page 13)
	01/24	1. Change R140,R143,R146,R149,R162,R163,R164,R165,R172,R190,R191,R192,R194,R198,R200,R201,R217,R218,R224,R244,R246,R331,R337,R338,R341,R343,R364,R365,R366,R367,R368,R369,R370,R371,R373,R375,R380,R390,R392,R399,R404,R41,R421,R423,R424,R425,R427,R433,R434,R467,R527,R528,R537,R538,R539,R540,R541,R553,R554,R555,R557,R558,R559,R568,R569,R570,R573,R587,R589,R590,R627,R637,R638,R644,R645,R646,R647,R657,R662,R668,R677,R678,R679,R680,R684,R685,R686,R687,R688,R689,R690,R691,R764,R765,R766,R767,R775,R777,R778 from 0 ohm to shortpad. (page 2~22)
	01/25	1. Modify BOARD_ID5 to Type-C function (page 13) 2. Change PR8009 from 100k ohm to 0 ohm. (page 27) 3. Change EMI capacitor C483 from 10p to 33p. (page 17) 4. Stuff R473 for EMI solution. (page 17)
	02/02	1. Change R115 from 0.0002 ohm to 0 ohm for the U22 power supply. (page 5)
	02/03	1. Change HOLE21 foot print to H-TBC236IC115D95P2. (page 17)
	02/06	1. Change HOLE15 foot print to H-C122D122N. (page 17) 2. Change HOLE4 foot print to HG-TC315BC236D95P2. (page 17)
	02/07	1. Change HOLE8, 9, 10, 11 foot print to H-C256IC146D146P2 (page 17)
	02/10	1. Change C183, C185 from 27pF to 33pF. (page 6) 2. Change C186, C187 from 6.8pF to 10pF. (page 6) 3. Change PR3021 from 24k ohm to 29.4k ohm for thermal requset. (page 30)
	02/15	1. Change PU8005 part number to AL005049000. (page 29)
	02/16	1. Change all the CH01006JBD1 to CH01006JB08. (page 4, 6, 7, 22)
	02/17	1. Stuff PC128 and PC8047 for noise issue. (page 24, 28) 2. Change PC164, PC166 from 10uF to 22uF for noise issue. (page 23) 3. Change R704, R705 from 0 ohm to 15 ohm for ESD solution. (page 21)
ZAV Rev. D RAMP-stage	02/20	1. Add C835 100pF for LCD flicker improvement. (page 15) 2. Add C836 0.1uF for enhance sensitive net ESD level by Intel suggestion. (page 9)
	02/28	1. Un-stuff SW1 power switch. (page 22)
	03/03	1. Un-stuff U35, U36 on RAMP build. (page 16) 2. Stuff R494, seting HDD redriver IC EQ2 7dB. (page 18) 3. Add R779, R780 for KabyLake R-U42 uesd. (page 9) 4. Change R115, R116 from 0 ohm to 0.0002 ohm. (page 5)
	03/06	1. Stuff C823 for eDP power supply input. (page 15) 2. Add R781 2.2 ohm for LID switch power supply. (page 15)
	03/07	1. Change R121,R122,R124,R126,R177,R227,R229,R230,R231,R232,R233,R234,R235,R236,R243,R245,R255,R278,R279,R280,R281,R290,R291,R292,R293,R374,R377,R384,R396,R398,R400,R411,R414,R460,R465,R469,R470,R473,R480,R490,R491,R492,R493,R501,R510,R523,R524,R525,R542,R543,R545,R552,R563,R564,R575,R581,R598,R640,R641,R643,R663,R671,R672,R675,R676,R714,R715,R716,R717,R718,R719,R720,R721,R733,R769 from 0 ohm to shortpad. (page 2~22) 2. Change power part PJ8000,PJ8001,PJ8002,PR8006,PR8009,PR8014,PR8016,PR8025,PR8029,PR8032,PR8035,PR8036,PR8038,PR8044,PR8045,PR8050,PR8051,PR8053,PR8056,PR8058,PR8074,PR8075,PR8077,PR8078,PR8080,PR8095,PR8097,PR8098,PR8113,PR8115,PR8116,PR8120,PR8121,PR8122,PR8079,PR8096,PR8114,PR8086,PR8088,PR8089,PR8087 from 0 ohm to shortpad. (page 23~31) 3. Non-stuff R58,R61,R542,R543 for RAMP stage. (page 4, 19)
	03/08	1. Non-stuff R108 for KabyLake U-U22 and R-U42. (page 5) 2. Add C837 0.1uF for intel ESD solution. (page 9)
	03/13	1. Change DRAM U9,U10,U11,U12 foot print to bga96-micron-mt41j64m16jt-187eg. (page 12)
	03/14	1. Swap U29 pin-1 and pin-9 for layout placement. (page 21) 2. Remove TP63 for layout placement. (page 21) 3. Remove R431, R434 EMI circuit for layout placement. (page 16) 4. Non-stuff C236, it can't power on with some 8GB or 16GB memory. (page 11)

 Quanta Computer Inc.		DOC NO.	PROJECT MODEL :		APPROVED BY:		DATE:
<div>File Document Number Rev. 1A</div> Change List - 2			PART NUMBER:		DRAWING BY:		REVISION:
Date: Wednesday, March 15, 2017							

